TECHNISCHE UNIVERSITÄT DARMSTADT — GSI — R3B — FAIR

HK 48.67

The NUSTAR Data Acquisition

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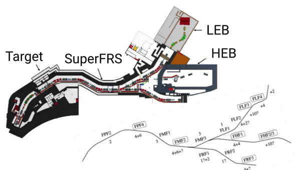
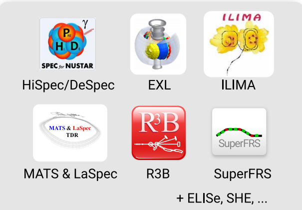
Overview

NUSTAR experiments @ FAIR





The challenge

9 large collaborations + common WGs
Total of > **80** individual detector systems
Total of > **200.000** detector channels
Total of ~ **1GB/s** data rate peak

NDAQ Requirements

Support all detector types and electronics
Correlate subsystems via timestamps
Handle high data throughput
Assure data integrity
Allow hybrid trigger schemes
Provide slow control and monitoring
Support future detector generations

Solution

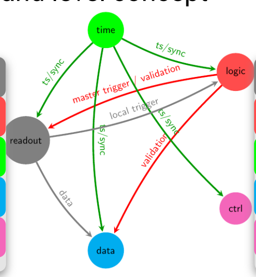
Common NDAQ infrastructure for all experiments
(i.e. common Trigger, Timestamps, Readout Control,...)
Distributed DAQ system with independent subsystems
Standard interfaces between subsystems
Appropriate **standard hardware**
Continuously running main components

Infrastructure

The NDAQ core and level concept

Cores specify capabilities of the underlying hardware

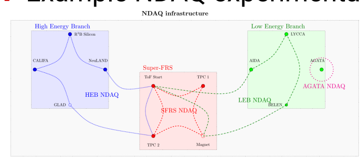
- Readout Core: Readout of detector system
- Logic Core: Process logic (trigger) signals
- Time Core: Time reference and clock sync
- Data Core: Event data flow / storage
- Control Core: Run control and slow control

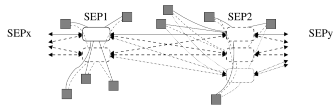


Cores interact on several interaction levels with each other

- Readout Level: Interface NDAQ <-> Subsystem
- Logic Level: Optical interconnects (direct)
- Time Level: Time/Clock network
- Data Level: High speed ethernet
- Control Level: Access to control cores

Example NDAQ experimental setup





3 experiments running in parallel
All nodes connected to NDAQ infrastructure
Experimental data is available everywhere and at all times

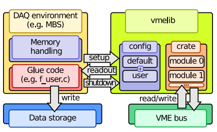
Signal exchange points (SEPs) allow **permanent** connection via logic signals
Setup is changed in software

Readout / Trigger

Generic readout library

Features Bus-based, written in ANSI C
Configurable using text files
Sane defaults are provided
Agnostic of DAQ environment
Support standard and fast transfer
Builtin logging/debugging
Online data integrity checks
Support multi-event mode

Overview



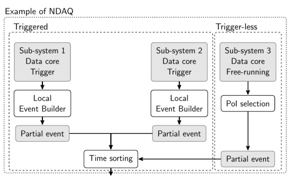
Example config file

```
CRATE("VME0", 0) {                # Name and crate ID
  multi event = true              # Use multi-event
  GSI_TRIDI(0x02000000) {}        # Type + address
  CAEN_V775(0x00010000) {
    common_start = true           # Setup parameters
    time_range = 1200 ns          # Support for units
  }
}
```

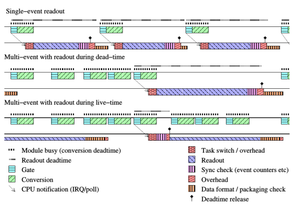
Operated since 2014 @ GSI, Duke University, RIKEN

Triggered **and** free-running

Hybrid mode is possible with timestamping/-sorting
Validation windows for free-running systems
Flexible FPGA Trigger Logic **TrLoII** (VULOM)
Easily scalable, just add NDAQ subsystems
Tested and operated in 2014 experiments @ Cave C

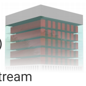


Single <-> Multi-Event



Data Storage

Data logging



Use Green Cube facility (FAIR IT)
Setup parameters in git tree
Control events written to data stream

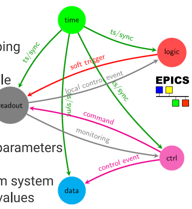
Sticky Control Events

Events containing settings affecting analysis
(i.e. accelerator/magnet settings, topology,...)
Time-ordered and ***sticky***
Automatic housekeeping vs. manual logbook
Only the data file is needed for analysis

Control

Run Control

Global control of data flow
Local control for starting/stopping subsystem
Attach/detach subsystems while running without full reset



Slow Control

Control/Monitoring of system parameters
Based on EPICS
Proper authentication and alarm system
Save/Restore of all parameter values

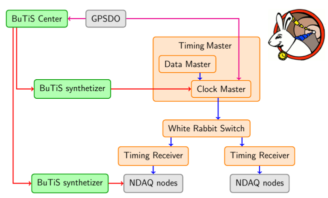
Timing / Synchronization

Rabbits

White Rabbit delivers absolute time reference on campus
Allow for timestamping of data and triggers
Time-sorting and merging of data from disjunct systems
Gray rabbit for systems without special hardware
Operated in experiments @ Cave C <-> FRS since 2012

BuTiS

Distributed phase-stable clock reference for synchronization
Enable high accuracy time measurements across campus



See also **HK 59.7** (Thu, 18:45), H. Törnqvist
HK 60.1 (Thu, 17:00), S. Paschalis
HK 51.1 (Thu, 14:30), K. Miki

Abstract — TRLOII — VMELIB — NUSTAR